Device Considerations and Modeling for the Design of an InP-Based MODFET Millimeter-Wave Resistive Mixer with Superior Conversion Efficiency

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Abstract—**We report on the device considerations for resistive FET mixer applications and discuss the design and fabrication of an optimized InP-based 0.1 μm gate length planar-doped pseudomorphic $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ modulation-doped FET (MODFET) well-suited for resistive mixer applications. In addition, we present a general large-signal model suitable for describing the FET in its passive mode of operation to assist in the design and simulation of such mixers. Finally, we discuss the theoretical design of a novel W-band, image-reject resistive mixer based on a large-signal model of our optimized device. The predicted performance of the mixer under +8 dBm of LO drive indicates a minimum conversion loss of 9 dB at 94 GHz, a significant improvement of over 3 dB in comparison to similar GaAs-based mixers, suggesting the potential of InP-based resistive mixer technology to achieve superior conversion loss performance.**

I. Introduction

THE CONTINUAL advancement of state-of-the-art III-V heterostructure FET-based low noise amplifiers and their incorporation into high performance receivers at microwave and millimeter-wave frequencies has prompted focus on other areas of the receiver subsystem in need of improvement. In particular, reduction in distortion and spurious responses of the mixer has become increasingly important. The resistive FET mixer topology has achieved prominence in low distortion mixing applications at microwave and millimeter-wave frequencies as evidenced by increased activity in the recent literature concerning the development of such mixers at millimeter-wave frequencies [1]–[3]. Resistive FET mixers have been shown to possess better intermodulation and compression performance in comparison to their diode-based counterparts, with similar LO power requirements, conversion loss, and noise performance [4]. Although GaAs-based resistive FET mixers have demonstrated low intermodulation distortion as well as good conversion loss and noise figure at microwave and millimeter-wave frequencies [5], [6], it is anticipated that InP-based resistive FET mixers will attain superior conversion efficiency at comparable levels of LO drive due to fundamental advantages provided by InP-based materials.

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In this paper, an analysis of the device requirements for low conversion loss resistive mixer applications is presented and a novel InP-based MODFET structure that possesses unique traits which, we claim, make it an ideal candidate for such applications is proposed. Experimental DC and RF results for a 0.1 μm gate length device are also presented, and illustrate the validity of the claims. In addition, the development of an empirically-derived, analytical, large-signal passive FET model useful for simulating the operation of a FET device at zero drain bias, and which has been successfully used to model our InP-based MODFET device, is discussed. Using this model, a 94 GHz image-reject mixer has been designed, and large-signal simulations indicate its capability to achieve a significant improvement in conversion efficiency of over 3 dB in comparison to state-of-the-art GaAs-based resistive mixers.

II. Device Considerations for Resistive FET Mixer Applications

In the resistive FET mixer topology, the FET device is operated in its common-source configuration and the LO is applied to the gate to modulate the channel conductance from pinch-off to fully conducting. The RF is applied at the drain, which is biased at zero volts, so that the varying channel resistance beats with the RF and generates a low frequency IF signal at the drain. Appropriate filtering is employed to extract the IF from the drain. Simply put, the FET device operates as a two-state dynamic switch controlled by the LO. The important parameters governing the operation of a dynamic switch are its ON- and OFF-state impedances, input control voltage swing, and transition time required to switch from ON to OFF and vice versa. An ideal switch has zero ON-state resistance, an infinite OFF-state impedance, and obviously, requires a minimal input voltage swing as well as zero time for transitions between these two states. Thus, the optimum device for resistive mixer applications is one which most closely approximates the characteristics of the ideal dynamic switch. This section discusses the parameters of the FET which are critical in determining its performance as a dynamic switch.

In the "switch" mixer, the time dependence of the impedance of a dynamic switch varied between ON and OFF states at the LO frequency may be described by a square-wave function, $S(t)$, which may be expressed as a Fourier

series, i.e.,

$$S(t) = \frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}} \cos n\omega_{\rm LO} t.$$

With an input RF signal, $V_{\rm RF}(t)$, in series with the LO-controlled dynamic switch, alternately allowing and preventing the RF signal to pass to the output, the output voltage, $V_O(t)$, is thus given by

$$\begin{aligned} V_O(t) &= V_{\rm RF}(t) \times S(t) \\ &= V_{\rm RF} \cos\omega_{\rm RF} t \left(\frac{1}{2} + \sum_{n=1}^{\infty} \frac{\sin\frac{n\pi}{2}}{\frac{n\pi}{2}} \cos n\omega_{\rm LO} t \right). \end{aligned} \quad (1)$$

From this equation, it is apparent that all even harmonics of $\omega_{\rm LO}$ will disappear from the output and there also will be no terms of frequency $\omega_{\rm LO}$ or its odd harmonics. Only terms due to the products of $\cos\omega_{\rm RF} t$ and $\cos n\omega_{\rm LO} t$ with n odd will exist. For downconverter applications, an intermediate frequency signal at $\omega_{\rm IF} \equiv \omega_{\rm RF} - \omega_{\rm LO}$ may be extracted at the output.

From (1), it is apparent that a two-tone input

$$V_{\rm RF}(t) = V_{\rm RF}(\cos\omega_{\rm RF1} t + \cos\omega_{\rm RF2} t)$$

generates no third-order intermodulation distortion (IMD) products at either $2\omega_{\rm RF1} - \omega_{\rm RF2} - \omega_{\rm LO}$ or $2\omega_{\rm RF2} - \omega_{\rm RF1} - \omega_{\rm LO}$ at the output. Since the *actual* FET channel resistance is nearly truly linear at low drain-source voltages, the excellent theoretical IMD performance of such mixers has been verified in practice where GaAs MESFET-based resistive FET mixers have exhibited input IP_3 intercepts over +30 dBm for an LO drive near +20 dBm [7].

Both the conversion loss and distortion performance of the resistive FET mixer are strongly dependent on the magnitude of the input LO drive voltage. The LO signal must swing the gate potential as quickly as possible from pinch-off at $V_G = V_{\rm th}$, to fully conducting, i.e., minimum channel resistance, at $V_G = V_f$. Thus, the minimum LO voltage swing required, $\Delta V_{\rm LO}$, is defined to be the difference between $V_{\rm th}$ and V_f, when the gate of the FET is biased such that equal excursions of the LO voltage above and below the bias point allow the device to turn ON and OFF, respectively, i.e., $\Delta V_{\rm LO} = V_f - V_{\rm th}$. The equivalent circuit of the LO port at the gate of the FET has been presented in [5], and the impedance at the LO port, $Z_{\rm LO}$, may be written as

$$Z_{\rm LO} = R_g + R_s \| R_d + \frac{1}{j\omega(\widetilde{C_{\rm gs}} + \widetilde{C_{\rm gd}})}. \quad (2)$$

Here, $\widetilde{C_{\rm gs}}$ and $\widetilde{C_{\rm gd}}$ are averages taken over the LO voltage swing. From (2), the expression for $P_{\rm LO,min}$ may be derived by considering the LO port to be conjugately matched. In this case, the minimum LO power required, or the time-averaged power dissipated at the gate input of the FET is defined to be

$$P_{\rm LO,min} = \frac{1}{2} {\rm Re}(\mathbf{V_G} \mathbf{I_G}^*)$$

where $\mathbf{I_G}$ represents the complex RF current into the gate input and $\mathbf{V_G}$ is the complex RF voltage at the gate terminal. These quantities are related to one another thru $\mathbf{V_G} \equiv \mathbf{Z_{LO}} \mathbf{I_G}$. Now, assuming the gate is biased near the midpoint between $V_G = V_{\rm th}$ and $V_G = V_f$, then

$$\mathbf{I_G} = \frac{\frac{\Delta V_{\rm LO}}{2}}{\frac{1}{j\omega(\widetilde{C_{\rm gs}} + \widetilde{C_{\rm gd}})}}. \quad (3)$$

Thus

$$P_{\rm LO,min} = \frac{1}{2} {\rm Re}(|\mathbf{I_G}|^2 \cdot \mathbf{Z_{LO}}) \quad (4)$$

$$= \frac{1}{2} \cdot \frac{\Delta V_{\rm LO}{}^2}{4} \cdot \omega^2 (\widetilde{C_{\rm gs}} + \widetilde{C_{\rm gd}})^2 \cdot (R_g + R_s \| R_d). \quad (5)$$

(5) suggests that a reduction in the minimum required LO voltage swing, $\Delta V_{\rm LO}$, helps to reduce $P_{\rm LO,min}$, implying that the threshold voltage of the FET should reside as near to zero as possible, e.g. the FET should be "nearly normally-off" or nearly enhancement-mode.

The finite transition time between ON- and OFF-states of a non-ideal switch leads to the existence of a finite interstate impedance. During this interstate switching time, the output voltage is related to the input voltage by a simple resistive divider, implying that the linearity of the interstate switch impedance affects the generation of distortion at the output. Thus, the transition time between the ON- and OFF-states of the FET should be minimized in order to reduce the distortion which may be generated by the weakly nonlinear resistance of the FET channel. This switching time is dependent on how sharply the FET's channel conductance increases to reach its fully conducting state, i.e., the amount of change in channel conductance per incremental step in gate voltage. A relation which describes the sharpness of the turn-on of a FET may be derived from the expression for the drain-source current, $I_{\rm DS}$, of a FET at low drain voltages given by

$$I_{\rm DS} = \left(\frac{W}{L} \right) q\mu_n V_{\rm DS} \cdot n_{\rm ch} \quad (6)$$

where μ_n is the electron mobility, and $n_{\rm ch}$ is the subthreshold channel electron density at the source. Now, the channel conductance, $G_{\rm ch}$, is given by

$$G_{\rm ch} = \frac{\partial I_{\rm DS}}{\partial V_{\rm DS}} = \left(\frac{W}{L} \right) q\mu_n \cdot n_{\rm ch}.$$

An approximation commonly used for $n_{\rm ch}$ as a function of gate voltage, V_G, is

$$q n_{\rm ch} = C_G (V_G - V'_{\rm th})$$

where C_G is the gate-to-channel capacitance per unit area and $V'_{\rm th}$ is the effective threshold voltage. Finally

$$\frac{\partial G_{\rm ch}}{\partial V_G} = \left(\frac{W}{L} \right) \mu_n \cdot C_G \quad (7)$$

is a relation which describes how quickly the FET may turn on. (7) suggests that achieving a quick turn-on requires a device with a high mobility near threshold.

The actual transition time of the FET switch is dependent on the LO drive power. This concept is illustrated in Fig. 1

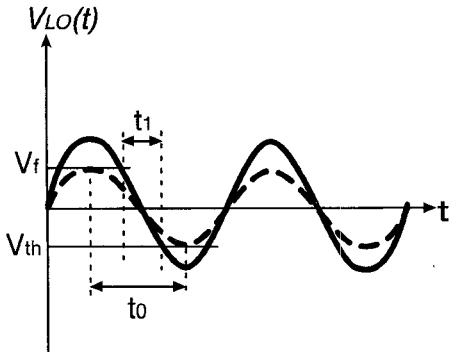


Fig. 1. Comparison of lower ('- - -') versus higher ('——') LO drive in relation to the transition time from device pinch-off to its fully-conducting state.

which represents an LO waveform in the time domain. One may observe that as the magnitude of the LO drive increases, a shorter period of time is required for transitions betwen the ON and OFF state thresholds delimited by V_f and $V_{\rm th}$, respectively, i.e., $t_1 < t_0$. Ideally, the higher the LO driving voltage swing, the shorter the transition time and hence the lower the harmonic distortion in the resistive mixer. However, in an actual FET device the Schottky-barrier gate has a limited forward dynamic range before significant gate junction leakage current arises due to the flow of hot carriers which may ascend and tunnel through the potential barrier between the metal and semiconductor. Since this gate junction possesses an exponential nonlinearity, excessive distortion is generated when the gate is driven into conduction, although the conversion loss of the mixer may be improved because of the increase in channel conductance due to the leakage current. These phenomena have been observed experimentally [5].

The minimum conversion loss, $L_{C,\min}$, attainable with resistive switch-type mixers may be estimated by the expression derived by Saleh [8], i.e.,

$$L_{C,\min} = 1 + 2\gamma^2\left[1 + \sqrt{1 + \left(\frac{1}{\gamma}\right)^2}\right] \tag{8}$$

where $\gamma \equiv \left|\frac{\mathbf{Z}_{\rm ON}}{\mathbf{Z}_{\rm OFF}}\right|$. (8) indicates that the ratio of the ON- versus OFF-state impedances of the FET determines its conversion loss. Maas has analyzed the equivalent circuit representation looking into the RF port of a resistive FET mixer [5], and from this analysis, the ON- and OFF-state impedances, $\mathbf{Z}_{\rm ON}$ and $\mathbf{Z}_{\rm OFF}$, respectively, may be written as

$$\mathbf{Z}_{\rm ON} \approx R_s + R_d + R_{\rm ds} \tag{9}$$

and

$$\mathbf{Z}_{\rm OFF} = R_d + \frac{1}{j\omega C_g} \approx \frac{1}{j\omega C_g}. \tag{10}$$

In (10) above, the value of the gate capacitance, C_g, is dependent on the nature of the termination for the RF frequency at the gate of the FET such that

$$C_g = \begin{cases} C_{\rm gd} & \text{if gate shorted at RF frequency} \\ \frac{C_{\rm gd}}{2} & \text{if gate open-circuited at RF frequency.} \end{cases} \tag{11}$$

Now, the channel conductivity, σ_s, of an FET is related to $R_{\rm ds}$ by the equation, $R_{\rm ds} = \frac{L}{\sigma_s W}$, and may be expressed as

$$\sigma_s = q\mu_n n_s \tag{12}$$

where L and W are the length and width of the FET gate, q is the electronic charge, μ_n is the electron mobility, and n_s is the free electron sheet density. The gate capacitance is related to the effective gate-to-channel separation, d, by the expression

$$C_g = \frac{\varepsilon}{d} L \times W \tag{13}$$

where ε is the permittivity of the semiconductor between the gate and channel. Thus, for the intrinsic FET, neglecting parasitic access resistances, R_s, R_d, and R_g, and using (12) and (13), the ON-OFF impedance ratio is given by

$$\gamma \equiv \left|\frac{\mathbf{Z}_{\rm ON}}{\mathbf{Z}_{\rm OFF}}\right| \propto \frac{\omega\varepsilon L^2}{q\mu_n n_s d}. \tag{14}$$

Referring to (8), to obtain minimum conversion loss, γ must be minimized. Thus, an FET device optimized for minimum conversion loss should have both a large μ_n and n_s, i.e., a high maximum channel conductivity, and a small gate capacitance, C_g. It is useful to note that although γ is independent of the FET gate width, the dependence of the expression for $P_{\rm LO,min}$ given in (5) on $\widetilde{C_{\rm gs}}$ and $\widetilde{C_{\rm gd}}$ implies that $P_{\rm LO,min}$ is directly dependent on the magnitude of the gate capacitance. This suggests that for resistive mixer applications, an appropriately sized device must be chosen for reasonable LO power requirements, particularly at higher frequencies. In addition, the impedance level of the device must be taken into consideration for matching purposes.

Since all FET's have similar drain I-V characteristics, to first order, the distortion performance of the resistive FET mixer is greatly dictated by its topology and the level of LO drive applied. On the other hand, the conversion efficiency of resistive FET mixers depends more strongly on specific device parameters. In summary, the important parameters of the FET which determine its performance as a dynamic switch-based mixer in terms of LO power required and conversion loss are its threshold voltage, the sharpness of its turn-on, and the maximum conductivity of its channel. To minimize the LO power required, (5) indicates that a device with a near enhancement-mode threshold voltage is desired. (7) also suggests that a high μ_n is also desired for quick device turn-on to help for minimum distortion as well as the LO power requirement. Finally, (14) implies that for low conversion loss, a device with a large mobility and high maximum sheet density is needed. In addition, the parasitic resistances should be minimized, implying that self-aligned gate FET technology should provide advantages [9].

Various GaAs-based compound semiconductor FET's, including the MESFET and MODFET, have been utilized in resistive FET mixer applications at many frequencies. Recently, an experimental investigation comparing the effect of different device structures on resistive FET mixer performance has been conducted and has indicated that a low-noise MODFET device achieved the best conversion loss with the lowest LO power requirement compared to uniformly- and planar-doped

MESFET devices [10]. The advantages of the MODFET over the MESFET in terms of conversion loss and LO power requirement are its improved channel transport properties, specifically its high channel electron mobility and velocity. These lead to a larger maximum channel conductivity and higher transconductances, allowing the MODFET to achieve high current densities with a near-zero threshold voltage. Although the MODFET originated on GaAs substrates using the venerable AlGaAs/GaAs heterojunction system, the superior electron transport properties provided by InP-based heterojunction systems have enabled InP-based MODFET's to jump to the forefront and become the foundation for the highest performance circuits in the microwave and millimeter-wave arena.

III. Experimental Results for an $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ on InP MODFET

To date, the best performing resistive FET mixers in terms of conversion loss have been fabricated utilizing pseudomorphic $Al_xGa_{1-x}As/In_yGa_{1-y}As$ on GaAs MODFET technology. Both hybrid and monolithic resistive mixers based on single- and double-heterojunction MODFET's have demonstrated the capability to achieve admirable conversion loss at frequencies approaching and exceeding 100 GHz. A further improvement in conversion loss performance is expected with the use of InP-based heterostructure materials since the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterojunction system which may be grown lattice-matched on InP possesses a larger conduction band discontinuity, ΔE_c, and smaller effective mass resulting in a significant increase in sheet carrier density and mobility and ultimately channel conductivity compared to the $Al_xGa_{1-x}As/In_yGa_{1-y}As$ on GaAs system. $In_{0.48}Al_{0.52}As/In_yGa_{1-y}As$ MODFET's with ($y > 0.53$) have exhibited the lowest noise figures and highest frequency figures of merit to date [9], [11], although an inherent problem has been the low gate-to-drain and channel breakdown voltages attainable with these devices. The low channel breakdown arises due to the small bandgap of the $In_yGa_{1-y}As$ ($y > 0.53$) material, although this is not much of a concern for resistive mixer applications since the drain of the device is typically grounded in order to maximize the swing of the small-signal RF voltage in the ohmic region of the drain characteristic to minimize distortion. However, low reverse gate-to-drain breakdown is caused by the low Schottky-barrier height of the $In_{0.48}Al_{0.52}As$ quasi-insulating layer, which is typically around 0.5 V [12]. This is also undesirable for resistive mixer applications since the large-signal LO voltage is applied to the gate of the FET, and may cause excessive forward gate leakage at high levels of drive, generating significant distortion due to the severe nonlinearity of the gate-channel diode junction.

A novel device structure which helps to overcome the problems associated with excessive gate leakage is the doubly-strained, planar-doped $In_xAl_{1-x}As/In_yGa_{1-y}As$ on InP MODFET, with $x < 0.52$ and $y > 0.53$. This device possesses the inherent traits which make it ideally suited for resistive mixer applications. In this device, both the barrier and channel layers are strained to maximize the ΔE_c and thus the maximum two-dimensional electron gas (2DEG) density which may accumulate in the heterojunction potential well. The higher molar fraction of indium incorporated into the channel minimizes the effective mass and consequently improves the mobility of electrons which reside in the channel layer, and the higher molar fraction of aluminum in the $In_xAl_{1-x}As$ barrier layer allows for an improved Schottky-barrier height [12]. Using the relations given in [13], a ΔE_c of 0.68 eV has been calculated for the $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ heterojunction, which is roughly 30 percent larger than for the lattice-matched case [14]. Initial investigations of doubly-strained $In_xAl_{1-x}As/In_yGa_{1-y}As$ heterojunctions on InP were carried out by Kuo *et al.* who demonstrated good performance of 1.7 μm gate length MODFET's [15], [16]. Recently, the transport properties of various modulation-doped $In_xAl_{1-x}As/In_yGa_{1-y}As$ heterojunctions, with $0.48 \leq x \leq 0.51$ and $y \approx 0.60$, have been studied. The results from the studies indicate that the strained $In_yGa_{1-y}As$ layers are pseudomorphic well beyond the critical thicknesses calculated by the Matthews-Blakeslee mechanical equilibrium model [17], [18].

In designing the doubly-strained device, the thicknesses of the strained layers were kept near the pseudomorphic limit predicted by the single-kink Matthews-Blakeslee model [19]. Starting from the semi-insulating InP substrate, the device layer structure for the $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET consists of a 2500 Å undoped $In_{0.52}Al_{0.48}As$ buffer, a 200 Å undoped $In_{0.53}Ga_{0.47}As$ pre-channel smoothing layer, a 150 Å undoped pseudomorphic $In_{0.65}Ga_{0.35}As$ channel, a 30 Å undoped pseudomorphic $In_{0.42}Al_{0.58}As$ spacer layer followed by a silicon planar-doping layer at 5×10^{12} cm^{-2} sheet density, a 200 Å $In_{0.42}Al_{0.58}As$ quasi-insulator and finally a 300 Å n^+ $In_{0.53}Ga_{0.47}As$ ohmic contact layer doped mid-10^{18} cm^{-3}. Hall-effect measurements made on the device structure with the n^+ ohmic contact layer removed showed a mobility of 8100 cm^2/V·s and a sheet carrier density of 2.9×10^{12} cm^{-2} at 300 K.

Devices with nominal gate lengths of 0.1 μm have been fabricated in our laboratory. Fig. 2 is a plot of the drain I-V characteristic for a 0.1×20 μm^2 device. The inset in Fig. 2 shows the typical region of operation for resistive FET mixer applications. For a drain bias in the conventional saturation region of operation for FET's at $V_D = 1.25$ V, the peak transconductance for the device is 880 mS/mm and the maximum drain current before significant forward gate conduction, $I_{DS,max}$, is over 850 mA/mm. An intrinsic f_t over 90 GHz has been extrapolated, and the device also has a low threshold voltage near $V_G = -0.4$ V, and exhibits good forward dynamic range, enabling +0.8 V to be applied to the gate before appreciable gate leakage, bettering the typical value of +0.4 V common to InAlAs/InGaAs on InP MODFET's. The improved forward gate swing is illustrated in Fig. 3, which plots the gate-source/drain junction current density versus voltage for the $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET compared to a similar lattice-matched $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MODFET structure. The improved Schottky barrier height of the pseudomorphic $In_{0.42}Al_{0.58}As$ quasi-insulating layer as well

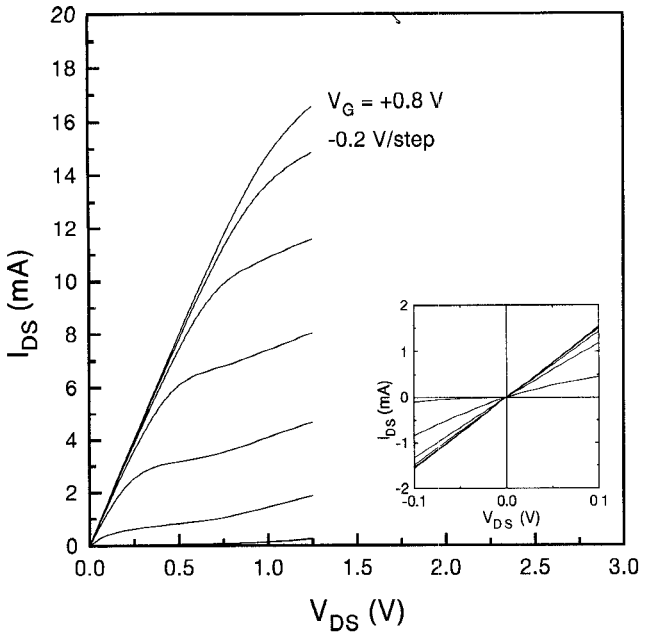


Fig. 2. Plot of I_{DS} versus V_{DS} for the 0.1×20 μm^2 $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET with inset showing typical region of operation for resistive FET mixer applications.

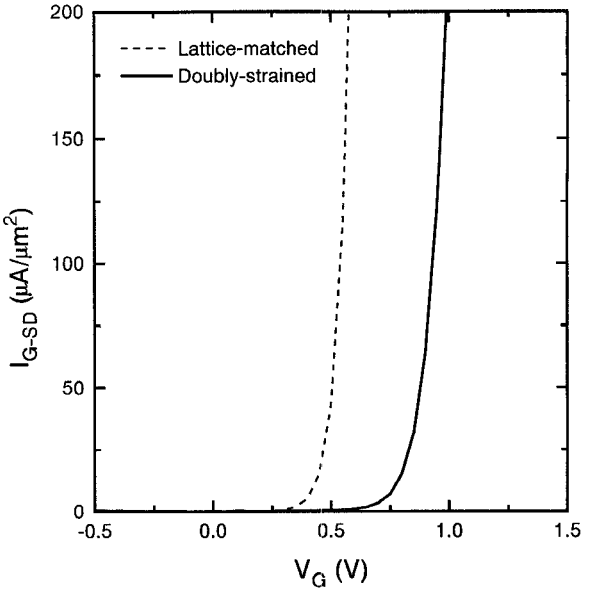


Fig. 3. Plot of I_{G-SD} versus V_G for both the lattice-matched $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ and doubly-strained $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET's.

as the large ΔE_c at the quasi-insulator/channel heterointerface, are both contributors to this forward dynamic range enhancement. In addition, the magnitude and broadness of the g_m versus V_G peak suggest efficient modulation and excellent confinement of the channel charge in the deep potential well at the front heterointerface, which help the device to simultaneously achieve both a high maximum current density and a near enhancement-mode threshold voltage. These are the parameters critical to resistive FET mixer performance and make the doubly-strained $In_{0.42}Al_{0.58}As/In_{0.35}Ga_{0.65}As$ MODFET an ideal candidate for such applications.

IV. Large-Signal Resistive FET Model

In this section, a nonlinear circuit model for the FET which accurately describes the operation of the device under zero drain bias conditions at millimeter-wave frequencies is presented. This region of operation is distinctly separate from the current saturation regime and the associated knee voltage of the drain I-V characteristic. The motivation behind the development of this type of model is due to the inability of "saturation region" large-signal FET models, such as the asymmetric Curtice-Ettenberg model [20], to comprehensively describe the operation of the FET in the linear region in order to accurately predict the conversion loss, gain compression, and distortion characteristics of resistive FET mixers.

Our large-signal model is based on empirically derived analytical expressions originally proposed by Plà and Struble [21] for both the channel conductance and gate-to-channel capacitances. The expressions rely on the tanh function to smoothly interpolate between the optimized small-signal parameters which are a function of gate bias. Angelov *et al.* have recently used a similar approach to model the nonlinear compression of the MODFET transconductance [22]. Our model additionally includes two nonlinear current sources

TABLE I
Optimized Small-Signal Parameters

Parasitic Elements		Intrinsic Elements							
			V_G (V)						
R_s (Ω)	20		−0.6	−0.4	−0.2	0.0	0.2	0.4	0.6
R_d (Ω)	25	C_{gs} (fF)	16 3	17.3	28.8	40 6	42 2	43 9	45 4
R_g (Ω)	13	C_{gd} (fF)	15 9	16.4	18.3	18 4	18 5	18.6	18 8
L_g (pH)	24	R_{ds} (Ω)	60000	8000	121	28.7	19.2	16.6	15.6
L_d (pH)	14	R_i (Ω)	14	14	14	14	14	14	14
L_s (pH)	1	C_{ds} (fF)	3	3	3	3	3	3	3

to account for the gate-drain and gate-source Schottky-diode forward junction currents which may flow when the gate is subjected to higher LO drive. This is particularly important for resistive mixer applications since the mixing mechanism of such mixers relies on a large LO input power at the gate to alternately switch the device on and off in order to generate the output IF signal at the drain.

To construct the large-signal model, bias dependent S-parameters were measured up to 40 GHz under zero drain bias and with a gate bias incrementally swept from pinch-off to the onset of forward gate leakage. The linear equivalent circuit shown in Fig. 4 was fit to the measured data at each bias point. Since the drain is biased at zero volts, the total gate-to-channel capacitance is more equally split between C_{gs} and C_{gd}. The procedure outlined in [23] was used to extract the capacitances from low frequency S-parameter data. A summary of the optimized equivalent circuit parameters is given in Table I. The dependence of the strongly nonlinear elements, C_{gs}, C_{gd}, and g_{ds} are plotted in Figs. 5 and 6.

The equivalent circuit for the large-signal model is shown in Fig. 4. The nonlinear elements of the model are C_{gs}, C_{gd}, and g_{ds}, which all vary with gate voltage. The expression

$$C(V_G) = C_0 \tanh\left((C_1 \times V_G + C_2) + C_3\right) \qquad (15)$$

where C_0, C_1, C_2, and C_3 are fitting parameters, has been used to model the dependence of both C_{gs} and C_{gd} on V_G, and

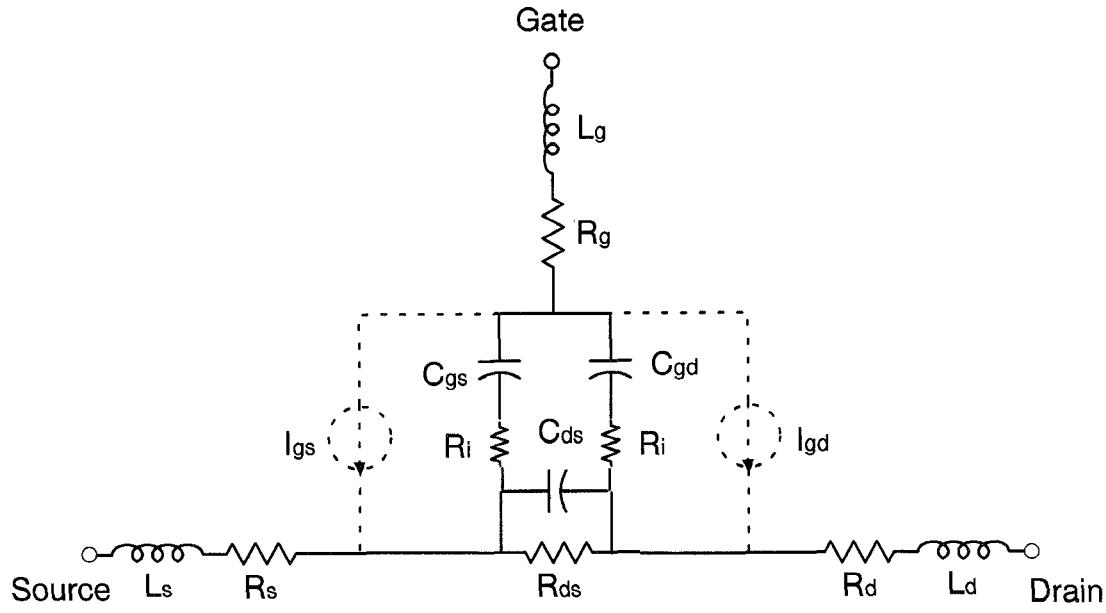


Fig. 4. Small- and large-signal equivalent circuits for the passive FET model with the large-signal model depicted through the inclusion of the gate-drain and gate-source current sources indicated as the dashed ('- - -') elements.

this model is represented as the dashed line in Fig. 5(a) and (b). A similar expression has been used to model the drain-source conductance, $g_{\rm ds}$, versus V_G, i.e.,

$$g_{\rm ds}(V_G) = g_0 \tanh\left((g_1 \times V_G + g_2) + 1\right) \tag{16}$$

where g_0, g_1, and g_2 are the fitting parameters. It is useful to note that the last argument of the tanh function in (16) has been set to 1 in order to prevent the conductance from becoming negative during parameter fitting. Fig. 6 plots both extracted and modeled $g_{\rm ds}$ versus V_G. The junction current, I_j, for the nonlinear current sources included at the gate-source and gate-drain junctions, is related to the junction voltage, V_j, by the expression

$$I_j = I_S\left\{\exp\left(\frac{qV_j}{nkT}\right) - 1\right\}, \tag{17}$$

where I_S is the reverse saturation current and n is defined to be the ideality factor. To model the total measured gate current, I_G, versus junction voltage, the gate-to-source junction current, $I_{\rm GS}$, is assumed to be equal to the gate-to-drain junction current, $I_{\rm GD}$, i.e., $I_G = I_{\rm GS} + I_{\rm GD}$. Fig. 7 plots the *total* measured and modeled nonlinear gate junction current.

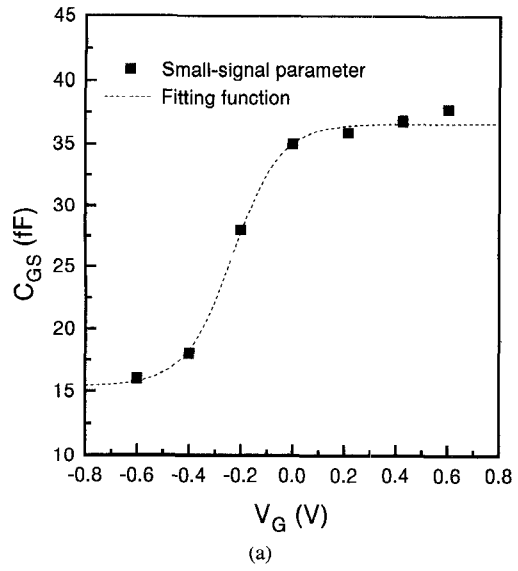
The parameters of the complete large-signal equivalent circuit for the $0.1 \times 20\ \mu\text{m}^2$ doubly-strained MODFET are given in Table II. The entire large-signal model has been implemented into EEsof's harmonic balance simulator, *Libra*, for use in the design and simulation of resistive FET mixer circuits. The model has already been used to model a 0.1 μm pseudomorphic GaAs-based MODFET to predict the performance of a W-band, monolithic singly-balanced resistive mixer. Simulations have shown reasonable agreement between simulated mixer performance and the measured results [6]. An example of simulated versus measured results is shown in Fig. 8, which illustrates how the simulated conversion loss compares favorably with measured data in predicting the saturation of conversion loss with increasing LO drive.

V. Image-Reject Resistive Mixer Design

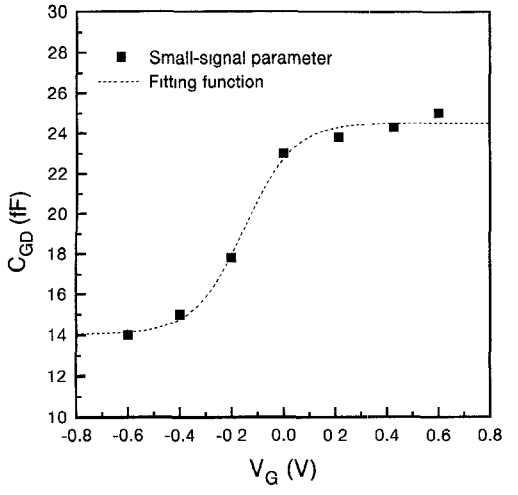
An image-reject resistive FET mixer was designed based on the large-signal model developed in the previous section for the $0.1 \times 20\ \mu\text{m}^2$ $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0\ 35}As$ MODFET. The mixer was designed for operation at an USB IF of 1.5 GHz over an RF band of 93.5–97.5 GHz with a corresponding LO band between 94–96 GHz. The topology of the mixer circuit is given in Fig. 9. Since the $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET device exhibited a near enhancement-mode threshold voltage, the mixer could be designed with no bias applied to the gates of the FET's without extracting a significant performance penalty in terms of LO power required. This helps to simplify and reduce the size of the circuit by avoiding the necessity of gate bias networks for both devices.

Using a Wilkinson power divider, an in-phase LO signal is injected into the gates of the FET's in order to swing the devices from pinch-off to fully conducting. The RF and IF signals are applied to and extracted from, respectively, the drains of the FET's through a diplexing filter. A Lange quadrature coupler is used to split the RF input power and to introduce a 90° phase shift between the RF signals at the two different drains. Since the LO and RF signals are applied at different ports of the FET's, separate matching networks may be included at the gates and drains to match the LO and RF inputs, respectively. This allows for good return losses at both input ports to be achieved. The impedance matching networks for the LO and RF and the low-pass filters for the IF are implemented using cascaded high and low impedance microstrip lines and MIM capacitors.

The predicted performance of the mixer was obtained through harmonic balance simulations using *Libra*. To obtain more accurate simulation results, the linear response of the Wilkinson power divider, the Lange coupler, and critical microstrip step discontinuities were modeled using Sonnet Software's *em* electromagnetic field analysis simulation tool,



(a)



(b)

Fig. 5. Extracted and modeled (a) $C_{gs}$and (b) C_{gd} versus V_G for the 0.1×20 μm^2 MODFET.

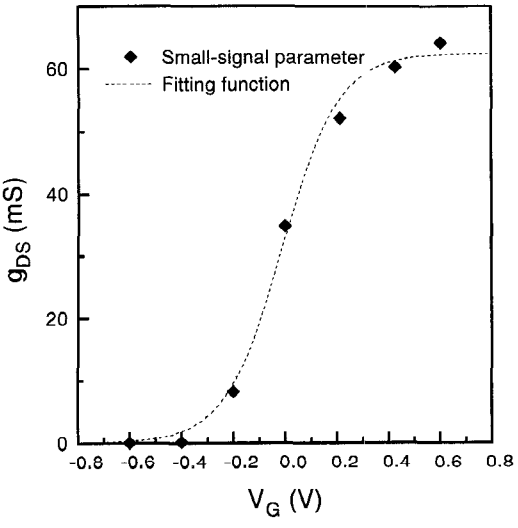


Fig. 6. Extracted and modeled g_{ds} versus V_G for the 0.1×20 μm^2 MODFET.

and the resulting S-parameters were used in the nonlinear simulations.

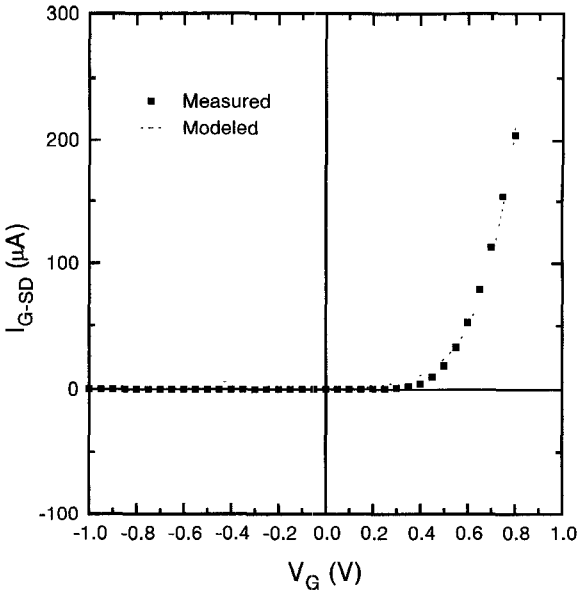


Fig. 7. Extracted and modeled I_{G-SD} versus V_G for the 0.1×20 μm^2 MODFET.

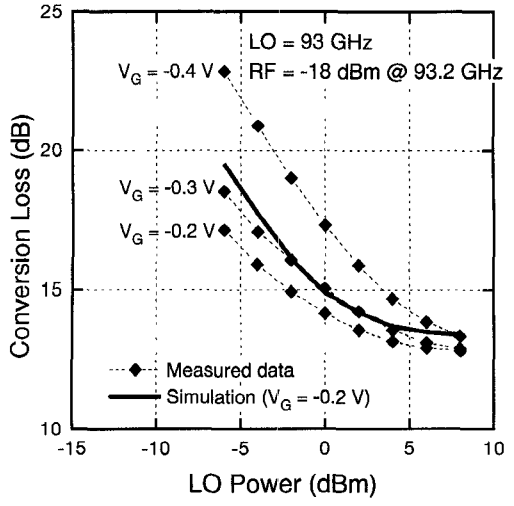


Fig. 8. Plot of conversion loss versus LO power for different values of gate bias.

First, the dependence of conversion loss on LO power is shown. In the simulations, the RF power was set to -20 dBm and the RF and LO frequencies were set to 94 and 92.5 GHz, respectively. Fig. 10 plots the conversion loss versus LO power. From this figure, the conversion loss appears to saturate near 10 dB for an LO power around $+6$ dBm, although the minimum conversion loss is 9 dB. A plot of the output IF power versus input RF power is shown in Fig. 11 for different levels of LO drive. At an LO power of $+6$ dBm, the input 1-dB compression point, $P_{1\text{-dB,in}}$, is near $+8$ dBm. Thus, this mixer exhibits similar compression characteristics compared to the measured performance of other resistive FET mixers [2], [6].

The simulated conversion loss and image-rejection across the LO band of 92–96 GHz are plotted in Fig. 12 for an LO drive of $+8$ dBm. From the simulations, the mixer has achieved a good image rejection of over 20 dB along with a flat conversion loss response. The minimum conversion

TABLE II
PARAMETERS OF THE LARGE-SIGNAL MODEL FOR THE $0.1 \times 20\ \mu m^2$ DOUBLY-STRAINED $IN_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET

Parameter	Value	Unit
C_{gs0}	10.60	fF
C_{gs1}	5.45	
C_{gs2}	1 26	
C_{gs3}	2.46	
C_{gd0}	5 24	fF
C_{gd1}	5.22	
C_{gd2}	0.79	
C_{gd3}	3 68	
g_{ds0}	31 2	mS
g_{ds1}	4.53	
g_{ds2}	0.05	
I_S	6.3×10^{-7}	A
n	4.5	

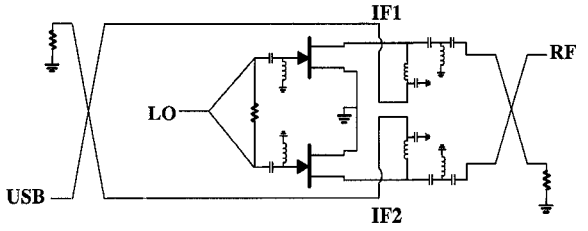


Fig. 9. Topology of the image-reject resistive FET mixer.

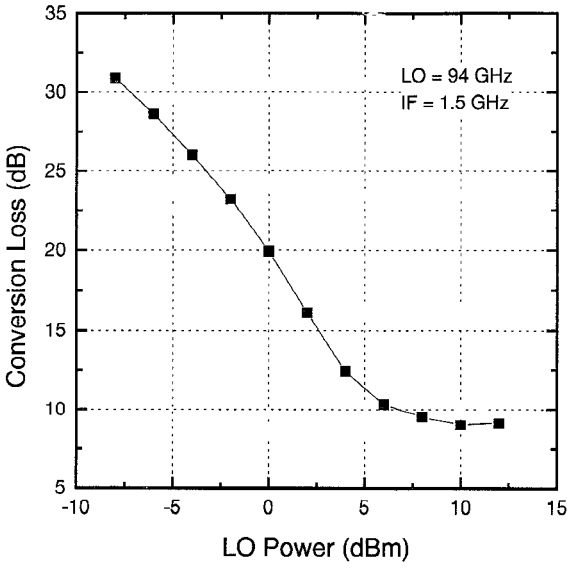


Fig. 10. Conversion loss versus LO power for the image-reject mixer.

loss of the mixer is near 9 dB at an LO drive of +8 dBm. This conversion loss performance is an improvement of over 3 dB in comparison to experimental data for GaAs-based resistive mixers in this frequency range [6], and is believed to be due to the higher maximum channel conductivity of the $In_{0.65}Ga_{0.35}As$ channel MODFET.

VI. CONCLUSION

The conversion efficiency and LO power requirement for the resistive FET mixer have been correllated with the physical parameters of a FET device. Specifically, the MODFET possesses the ideal traits for designing

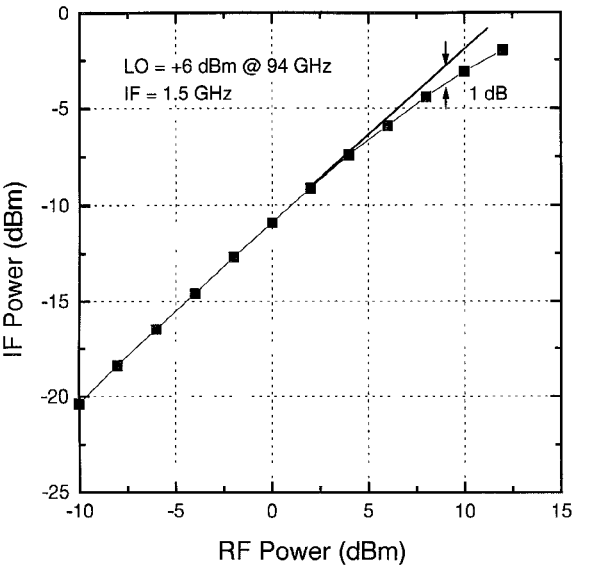


Fig. 11. Output IF power versus input RF power for the image-reject mixer.

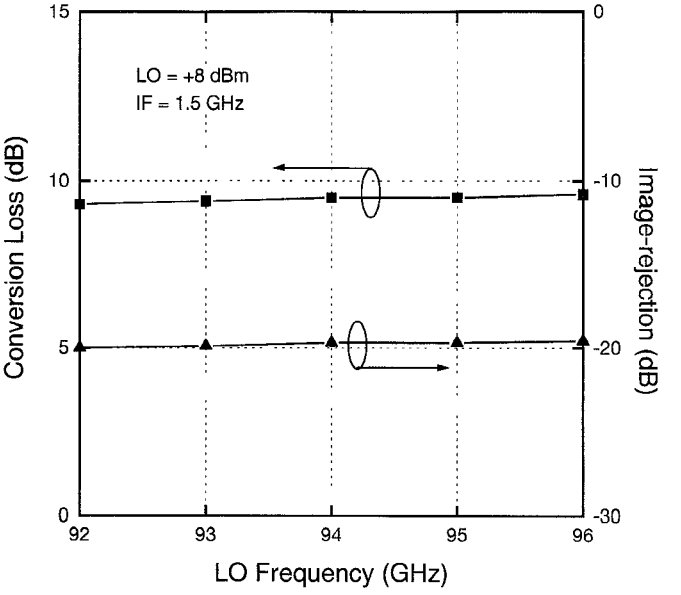


Fig. 12. Conversion loss and image-rejection versus LO frequency over the RF band of the image-reject mixer.

resistive mixers with low conversion loss and a minimum LO drive requirement. A 0.1 μm gate length doubly-strained $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ on InP planar-doped MODFET well-suited for millimeter-wave resistive FET mixer applications has been designed, fabricated and characterized in our laboratory. The doubly-strained MODFET has exhibited improved forward dynamic range and a high maximum current density, a result of the larger Schottky-barrier height of its strained quasi-insulator as well as the excellent confinement provided by the deep potential well created by the large ΔE_c at the $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ heterointerface.

To model the MODFET in its passive mode of operation, a general, empirically-based, analytical large-signal FET model has been developed which has proven useful in predicting the trends in conversion loss and IMD dependencies on LO power for resistive FET mixers. Using the large-signal model presented, the simulated performance of a monolithic

resistive FET mixer circuit has demonstrated good agreement in comparison to measured results.

Based on the large-signal model for the 0.1 μm gate length $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET, an image-reject resistive mixer has been designed for operation at 94 GHz. The topology of the mixer is well-suited for monolithic implementation and its simulated conversion loss performance demonstrates its excellent potential for use in wide dynamic range mixing applications at W-band frequencies. In addition, the mixer was designed completely unbiased without a significant penalty in conversion loss and LO power required due to the low threshold voltage and improved forward dynamic range of the $In_{0.42}Al_{0.58}As/In_{0.65}Ga_{0.35}As$ MODFET. Without bias circuitry, the complexity and ultimately the size of the circuit is reduced. Although the resistive FET mixer topology dictates its compression as well as its low distortion mixing characteristics, the improved conversion loss performance of the InP-based resistive FET mixer arises because of the lower minimum channel resistance attainable by MODFET's with larger ΔE_c's and channels of higher indium molar fractions, such as those which may be grown on InP.

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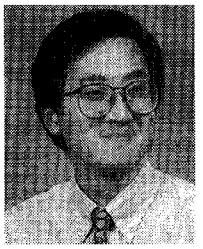

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